CLAIMS

1. An apparatus for providing measured power transitions in a computing device, the apparatus comprising:

   power control logic, configured to determine if the computing device is to enter a low power state, said power control logic comprising:

   a plurality of stop signals, each of said plurality of stop signals sequentially indicating that a corresponding clock signal be stopped, wherein said corresponding clock signal is operatively coupled to a corresponding sector logic element within the computing device.

2. The apparatus as recited in claim 1, wherein said each of said plurality of stop signals indicates that said corresponding clock signal be stopped after a programmable number of clock cycles.

3. The apparatus as recited in claim 2, wherein said programmable number of clock cycles is established for said each of said plurality of stop signals.

4. The apparatus as recited in claim 2, wherein said programmable number of clock cycles is the same number of clock cycles for said each of said plurality of stop signals.

5. The apparatus as recited in claim 1, further comprising:

interval logic, coupled to said power control logic, configured to provide a programmable number of clock cycles to said power control logic, whereby said power control logic causes said each of said plurality of stop signals to indicate that said corresponding clock signal be stopped after said programmable number of clock cycles.

6. The apparatus as recited in claim 5, wherein said interval logic comprises a register.

7. The apparatus as recited in claim 6, wherein said programmable number is provided by executing an instruction to program said register.

8. The apparatus as recited in claim 6, wherein said programmable number is provided by setting the state of fuses, said fuses being coupled to said register.

9. A power transition management mechanism, comprising:

interval logic, for providing one or more programmable numbers of clock cycles; and

power control logic, coupled to said interval logic, for receiving said one or more programmable numbers, and for employing said one or more programmable numbers to sequentially stop each of a plurality of clock signals that are coupled to each of a corresponding plurality of sector logic elements.

10. The power transition management mechanism as recited in claim 9, wherein said power control logic sequentially stops said each of a plurality of clock signals by asserting a corresponding each of a plurality of stop signals, wherein said each of a plurality of stop signals indicates that said each of a plurality of clock signals be stopped after a number of clock cycles have transpired, wherein said number is based upon said one or more programmable numbers.

11. The power transition management mechanism as recited in claim 10, wherein said one or more programmable numbers is established for said each of a plurality of stop signals.

12. The power transition management mechanism as recited in claim 10, wherein said one or more programmable numbers is the same for said each of a plurality of stop signals.

13. The power transition management mechanism as recited in claim 9, wherein said interval logic comprises a register.

14. The power transition management mechanism as recited in claim 13, wherein said one or more programmable numbers are provided by executing an instruction to program said register.

15. The power transition management mechanism as recited in claim 13, wherein said one or more programmable numbers are provided by setting the state of fuses, said fuses being coupled to said register.

16. An method for providing measured power transitions in a computing device, the method comprising:

determining if the computing device is to enter a low power state; and

sequentially stopping clock signals that are coupled to each of a plurality of sector logic elements.

17. The method as recited in claim 16, wherein said sequentially stopping comprises:

via each of a plurality of stop signals coupled to each of the plurality of sector logic elements, indicating that a corresponding one of the clock signals be stopped after a programmable number of clock cycles have transpired.

18. The method as recited in claim 17, wherein said indicating comprises:

establishing the programmable number of clock cycles for the each of the plurality of stop signals.

19. The method as recited in claim 17, wherein said indicating comprises:

establishing the same programmable number of clock cycles for the each of the plurality of stop signals.

20. The method as recited in claim 16, further comprising:

providing a programmable number of clock cycles that are to transpire between said stopping of the clock signals.

21. The method as recited in claim 20, wherein said providing comprises:

programming the programmable number of clock cycles into a register.

22. The method as recited in claim 21, wherein said providing comprises:

executing an instruction to accomplish said programming.

23. The method as recited in claim 21, wherein said providing comprises:

reading the states of fuses to accomplish said programming.